An FDTD–Touchstone Hybrid Technique for Equivalent Circuit Modeling of SOP Electronic Packages

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***Abstract*—The electromagnetic-field behavior within electronic packages used for high-speed digital-circuit or high-frequency analog-circuit applications often cannot be accurately modeled by using a quasi-static approximation, and a frequency-dependent analysis is sometimes needed for accurate modeling. In this paper, we employ the finite-difference time-domain (FDTD) approach, in conjunction with the commercially available software called Touchstone, to model the generic 24-pin silicon on plastic (SOP). The model for the package includes many details, such as the plastic encasement, bonding pads, and wires. The frequency responses of the package are tested against the results obtained with only the FDTD algorithm. It is shown that by extracting the equivalent-circuit elements from the field data, the hybrid FDTD–Touchstone technique allows greater flexibility in deriving a circuit configuration at the expense of fine tuning the circuit to reproduce the response of the package. It is hoped that the technique presented in this paper will lead to more accurate circuit simulations of complex packaging configurations than has been possible up to this point, by using quasi-static analyses.**

***Index Terms*—Electronic packaging, equivalent circuits, FDTD, silicon on plastic (SOP) package.**

I. Introduction

THE electromagnetic characterization of electronic packages containing high-speed digital or high-frequency analog circuits is of great practical interest [1]–[11], [14], and often these packages cannot be modeled accurately by using the quasi-static approximation. The methodology that is typically employed for modeling electronic packages entails the following steps.

1) The package geometry is subdivided such that it is manageable to model by using quasi-electrostatic and quasi-magnetostatic analysis tools which ignore the coupling between the electric and magnetic fields.
2) The equivalent capacitance and inductance are determined separately for each subsection, and the coupling between these subsections is ignored.
3) The lumped circuits are connected together to develop an equivalent-circuit package configuration, which can be inserted into a circuit simulator.
4) The model is adjusted on an as-needed basis to match the available measurements.

The finite-difference time-domain (FDTD) method [10]–[13] is a general-purpose Maxwell solver which is well-suited for modeling the frequency-dependent behavior of electronic packages. The field solution can in turn be used to generate an equivalent circuit comprising self and mutual inductances and capacitances, as well as resistances and conductances, in a form that can be directly inserted into a circuit simulator such as SPICE. Since the integrated-circuit chip typically contains many components, it would be very time consuming to accurately model all of them using the FDTD method described in [11]. In this paper, we investigate the problem of extracting such an equivalent circuit of a generic silicon-on-plastic (SOP) package shown in Fig. 1(a), by employing the full-wave solver FDTD method, in conjunction with the commercially available software Touchstone [14].[1]

In Section II, the package model will be described. In Section III, the equivalent circuits will be given for four different bond-wire configurations of the package. In Section IV, the equivalent circuits generated by using Touchstone will be presented and validated by demonstrating that their frequency response approximates that directly computed via FDTD method in the frequency range of interest.

II. Modeling the SOP Package

The first step in analyzing the SOP package, shown in Fig. 1(a) and (b), is to generate a mesh or a discretized model that describes the geometry of the package. A uniform-grid FDTD approach is used, and the unit cell size is chosen to be 0.0254, 0.0500, 0.0500 mm along the x-, y-, and z-directions, respectively, to ensure adequate spatial resolution. The entire computational domain consists of (181 $\times$ 176 $\times$ 30) cells. The physical size of the computational volume is about 4.6 $\times$ 8.8 $\times$ 1.5 mm^3, and symmetry is used where possible to reduce the size of the computational domain. To simplify computations and for purposes of illustrating this approach, the mesh is truncated with first-order Mur absorbing-boundary

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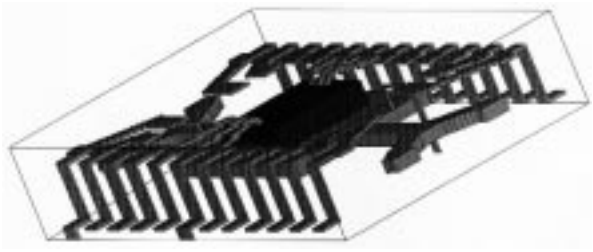
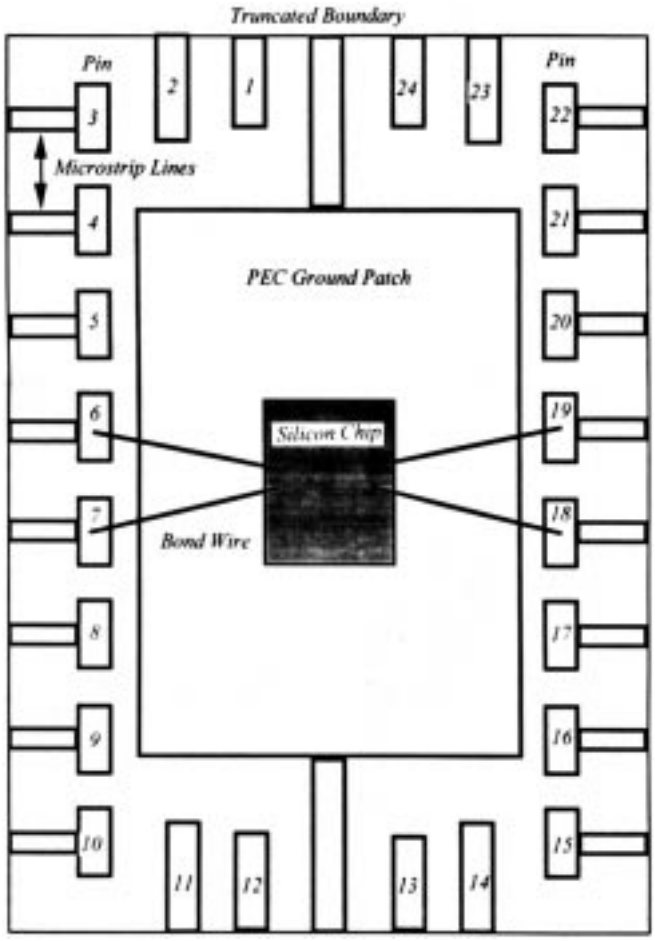
[1] Touchstone, EEsof Inc., Westlake Village, CA 91362.



(a)

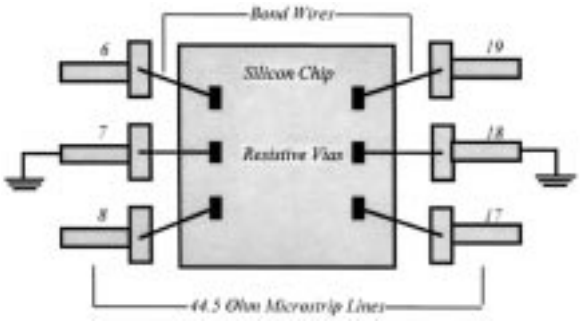


(b)

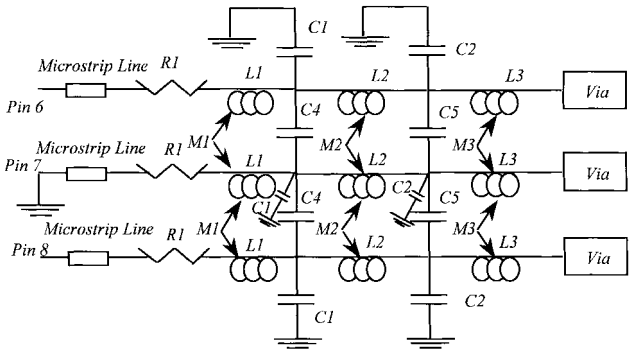
Fig. 1. (a) View of SOP package with substrate, modular plastic material, and PEC ground for microstrip lines removed. (b) Top view of the silicon chip with truncated boundaries.

conditions (ABC's) except at the symmetry planes where it is truncated with walls that are either perfect electric conductors or perfect magnetic conductors. More accurate ABC's which produce less reflections can be employed as described in [11], [13], and [15]. Based on estimating techniques as presented in [13], this model requires at least approximately 55 Mbytes of memory assuming 8 bytes of storage per field component and 1 byte per material parameter, and the upper estimate on the run time is roughly 10 central processing unit (CPU) h on a 50-megaflop (MFLOP) machine with additional run time included for any resonances that may occur.

As shown in Fig. 1(a) and (b), there are 12 pads or pin's along each side of the silicon package. In Fig. 1(a), the plastic



(a)



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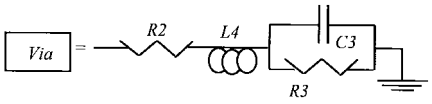


(c)

Fig. 2. (a) Input–output ports and terminations of silicon-chip package for Case A. (b) Equivalent circuit of the package derived by using Touchstone. (c) Circuit used to terminate vias.

material enclosing the package and microstrips connecting the package to the outside world has been removed to reveal the pin's or pads; however, it is included in the FDTD simulations. The plastic, which has a permittivity of 4.8, encloses the package such that only parts of the pin's are exposed to the outside. These pin's are shaped in the form of steps and provide solder points to circuitry outside of the package and bond wires inside. For the cases studied in this paper, the pin's are connected to 45-Ω microstrip lines on a grounded substrate characterized by a relative permittivity of 4.6.

A silicon chip whose permittivity is 11 is located on a finite-size perfectly conducting ground patch that acts as a virtual ground for the devices on the silicon, and is connected to the universal ground by vias, other virtual ground pads, and/or one or more bond wires, and pin's. The bond wires connect the patch to the pin's, which in turn are directly connected to the circuit board or universal ground through perfectly conductive vias. This ground is termed virtual, since as will seen later, the path from the patch to the universal ground contains significant inductance which must be included in the equivalent-circuit model.

For the various two-port configurations that will be analyzed, bond wires connect the appropriate input and output pads to the desired locations on the silicon chip. To form a complete path for current to flow from the microstrips outside

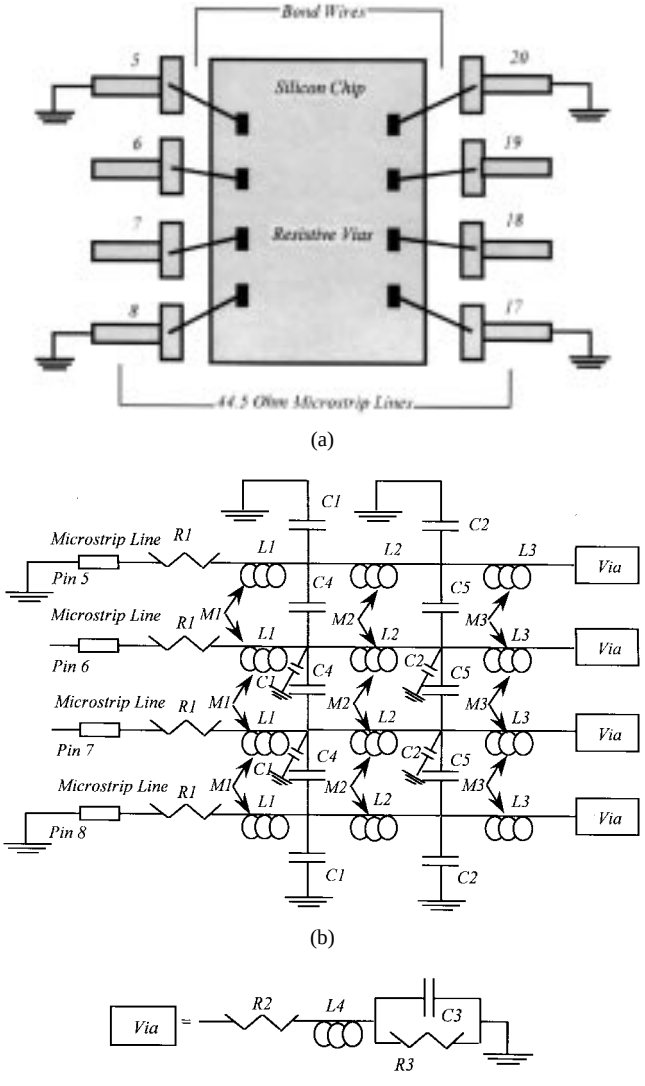


Fig. 3. (a) Input–output ports and terminations of silicon-chip package for Case B. (b) Equivalent circuit of the package derived by using Touchstone. (c) Circuit used to terminate vias.

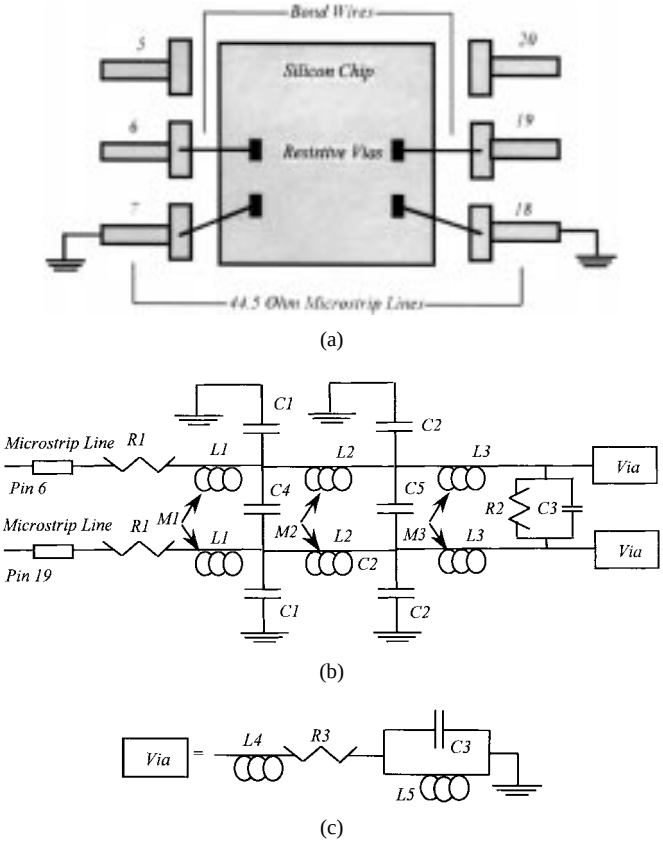


Fig. 4. (a) Input–output ports and terminations of silicon-chip package for Case C. (b) Equivalent circuit of the package derived by using Touchstone. (c) Circuit used to terminate vias.

of the package to the virtual ground, resistive vias connect the ends of the bond wires on the silicon chip to the virtual ground.

III. FDTD Analysis and Extraction of the Equivalent Circuits

The FDTD–Touchstone methodology employed to obtain the equivalent circuits of the four SOP package configurations will be described in this section, which will be followed in the following section by the analysis of the frequency response of the optimized equivalent circuits. Each circuit has four accessible nodes, two of which correspond to the bond-wire connections on the silicon and the remaining two correspond to the input and output terminals of the package. The goal of this approach is to develop accurate equivalent circuits that are based on a given circuit topology and that can be directly inserted into SPICE simulations of devices in the package.

To obtain the equivalent-circuit models, an approach similar to that described in [10] is employed. First, the FDTD algorithm is applied to compute the time-domain response of the package at the external input and output ports. The input port is excited with a suitable pulse, the time-domain responses of the package at both the input and output ports are computed by using the FDTD, and the scattering or S-parameters are extracted from these results.

Ideally, the S-parameters would be computed at all four ports instead of just the two external ports. However, this requires access to information on both the incident and reflected waves from the FDTD data at each port. To obtain this, a small section of matched microstrip line needs to be inserted at each port to record the incident and reflected traveling-wave responses at that port. This step is readily implemented for the external ports but is somewhat difficult to carry out at the internal ports due to the smallness of the chip size and the physical as well as electrical proximity of the bond-wire connections. One might attempt to circumvent this difficulty by using the FDTD method to directly compute alternative parameter sets such as the Z-parameters. However, this approach also presents problems because it is difficult to remove the effects of external impedances connected to the ports, e.g., the vias or microstrips.

In lieu of the internal port S-parameter data, the internal ports are handled by basing the equivalent circuit, which consists of resistors (R's), inductors (L's), and capacitors (C's) on the physical-package characteristics—for instance, self and mutual inductances are used to model the bond

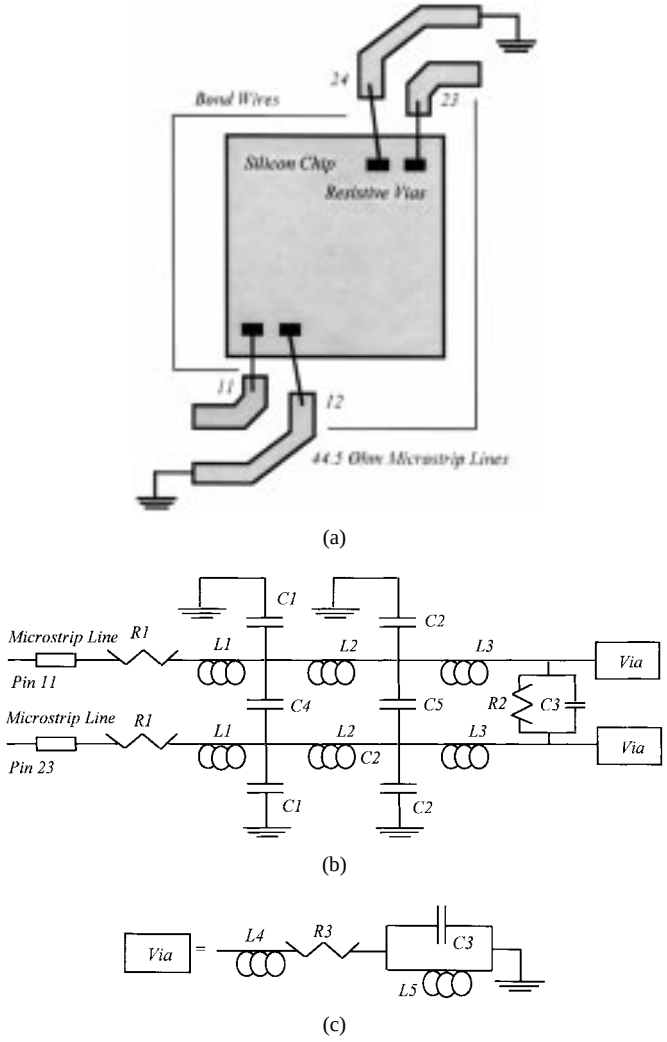


Fig. 5. (a) The input–output ports and terminations of silicon-chip package for Case D. (b) Equivalent circuit of the package derived by using Touchstone. (c) Circuit used to terminate vias.

wires. This circuit is subsequently optimized and tuned until its response, quantified in terms of its S-parameters at the external ports, matches that derived for the package by using the FDTD method. In the process of developing the circuit, the nodes which correspond to the internal ports or the connections on the silicon are included, hence, all four ports are available in the circuit model. The resultant circuits are given in Sections III-A and III-B.

The equivalent circuits presented below will be divided into two categories: "strong" and "weak" coupling circuits, which are based on the level of coupling between the input and output ports. Since the ports for the strong coupling case are in close proximity of each other, circuits with mutual inductance terms are used to describe their behavior. For the weak coupling circuits, the ports are far apart so the circuits with no mutual inductance terms are sufficient.

A. Strong-Coupling Cases

Case A: Pin's 6 and 8

For this configuration, a two-port network is defined with pin's 6 and 8 as the input and output ports, respectively, while pin's 7 and 18 are grounded. The physical model and the equivalent circuit for this case are given in Fig. 2(a)–(c).

TABLE I
LUMPED-CIRCUIT PARAMETERS COMPUTED WITH Touchstone
(UNITS ARE IN PICOHENRY, PICOFARAD, AND OHM)

Element	699.950
Case A	406.691
Case B	699.950
Case C	406.691
Case D	
L1	R1
998.864	48.191
998.864	48.931
597.093	44.265
495.711	29.172
L2	R2
735.467	40.078
735.467	0.268
701.128	42.000
358.926	28.500
L3	R3
101.886	65.537
101.886	129.212
104.856	6.168
348.157	1.231
L4	C1
66.582	14.390
19.294	14.390
258.409	4.832
430.868	12.568
L5	C2
	554.925
	554.925
388.793	654.940
5.523	4.406
M1	C3
699.843	30.859
943.046	44.562
0.011	48.012
	4.620
M2	C4
699.998	188.078
1199.000	399.970
793.808	318.207
	1.065
M3	C5
48.729	221.825
	279.777
	191.780
	3.070

Case B: Pin's 6 and 7

In this configuration, a two-port network is defined with pin's 6 and 7 as the input and output ports, while the pin's 5, 8, 17, and 20 are grounded. The schematic of the physical layout and the equivalent circuit are shown in Fig. 3(a)–(c).

Since the pin's 6 and 7 basically form a coupled transmission line, the output response at pin 7 due to the excitation at pin 6 has two contributions, which are the signal that travels from pin 6 to the silicon chip and back to pin 7 and the signal that directly couples to pin 7 from pin 6. In view of this, it is necessary to employ the following two linearly independent sources to excite the system: (+1 V, +1 V) and odd mode (+1

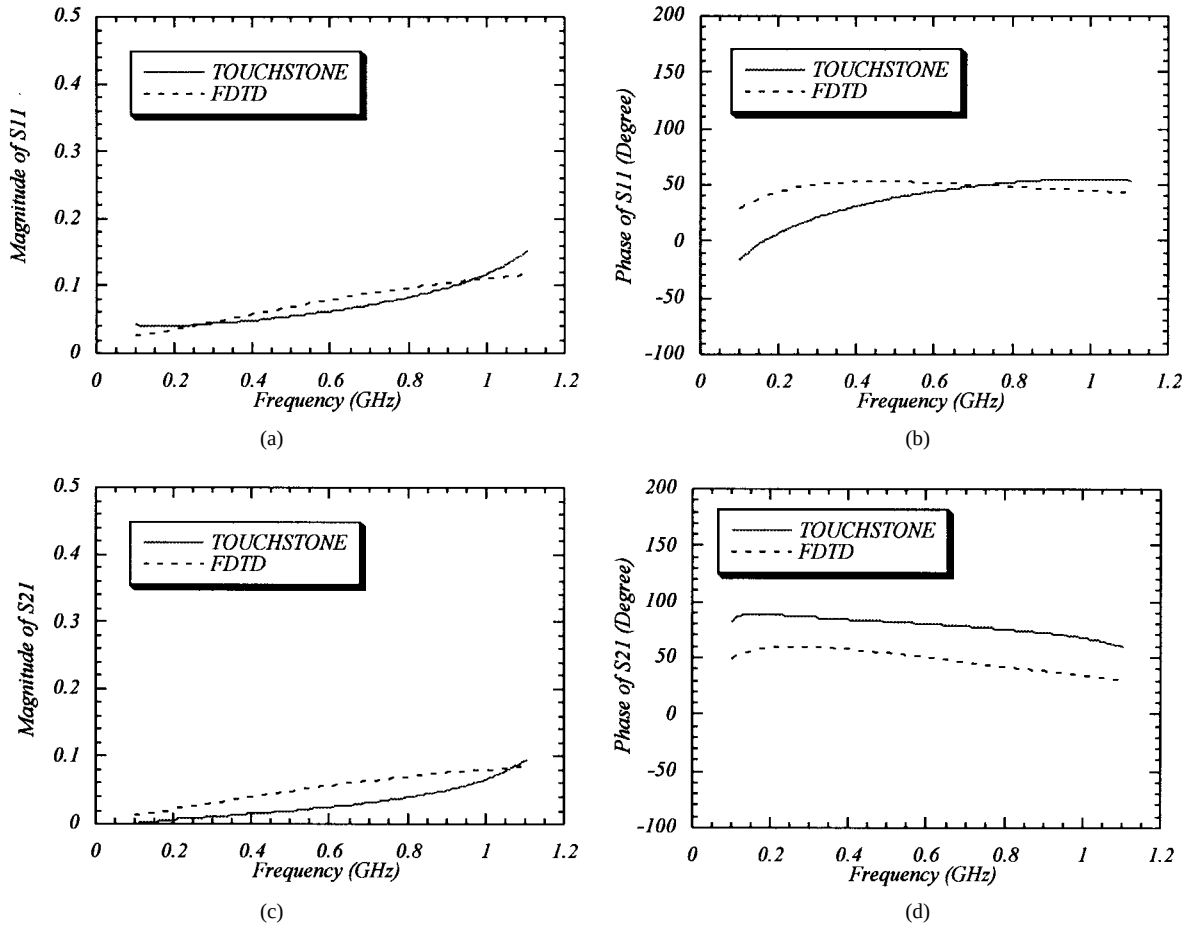


Fig. 6. (a) Magnitude of S_{11} of Case A. (b) Phase of S_{11} of Case A. (c) Magnitude of S_{21} of Case A. (d) Phase of S_{21} of Case A.

V, −1 V) to obtain the S-parameters S_{11}^{e} and S_{11}^{o}, respectively. Next, the S-parameters of the original two-port configuration are obtained via the following equations:

$$S_{11} = (S_{11}^{e} + S_{11}^{o})/2 \tag{1}$$

$$S_{12} = (S_{11}^{e} - S_{11}^{o})/2 \tag{2}$$

where the superscripts e and o represent the even and odd modal S-parameters of the modal system. Finally, the equivalent circuit is extracted from the S-parameters in the conventional way, utilizing the symmetry of the structure in this process that leads to the result $S_{22} = S_{11}$ and $S_{21} = S_{12}$.

B. Weak-Coupling Cases

Case C: Pin's 6 and 19

In this configuration, the two-port network is defined with pin's 6 and 19 as the input and output ports, respectively, and pin's 7 and 18 grounded. The physical layout and the equivalent circuit are shown in Fig. 4(a)–(c).

Case D: Pin's 11 and 23

In this configuration, the two-port network consists of pin's 11 and 23 as the input and output ports, respectively, while pin's 12 and 24 are grounded. The physical layout and the equivalent circuit are shown in Fig. 5(a)–(c).

IV. Scattering Parameters

The optimized equivalent circuits are checked by comparing the S-parameters derived from the equivalent circuits, with those computed from the FDTD analysis. The S-parameters are shown in Figs. 6(a)–9(b), with Fig. 6(a)–(d) showing both the magnitudes and phases of S_{11} and S_{21} for Case A. It is observed that the plots for the magnitudes of the two sets of S-parameters exhibit a better agreement with each other than do their phases. One explanation for this difference between the behaviors of magnitudes and phases might be as follows. During the optimization procedure of Touchstone, a small perturbation of the magnitude sometimes introduces a substantial variation in the phase data, i.e., the phase-variation is considerably more sensitive than the magnitude. The effect of the phase discrepancies in the scattering parameters obtained from the circuits on the SPICE simulation needs further investigation which is beyond the scope of this paper.

In the course of this project, an in-house algorithm was investigated for generating equivalent circuits for some of the electronic-package configurations in lieu of the equiv-

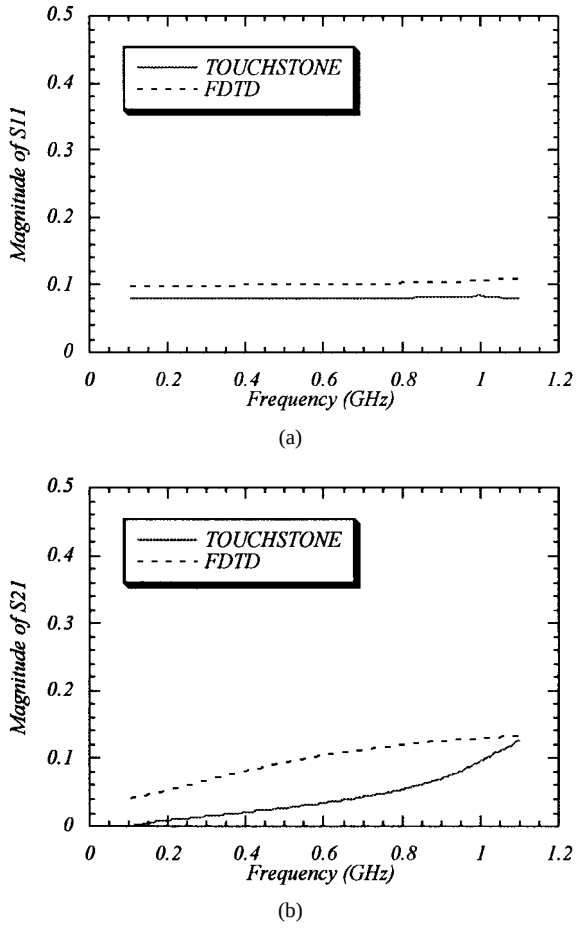


Fig. 7. (a) Magnitude of S_{11} of Case B. (b) Magnitude of S_{21} of Case B.

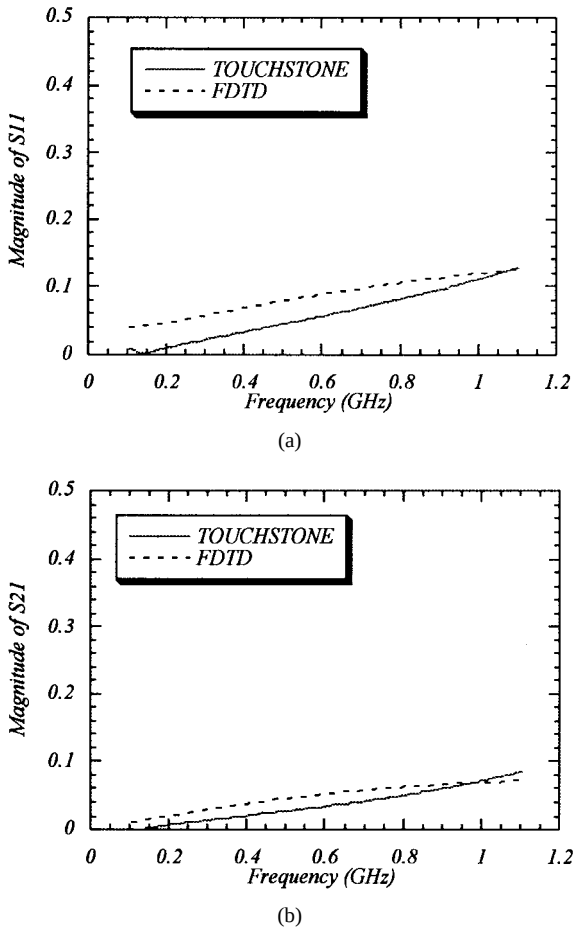


Fig. 8. (a) Magnitude of S_{11} of Case C. (b) Magnitude of S_{21} of Case C.

alent circuits presented here, which were developed based on physical-package considerations. Briefly, the algorithm provided equivalent circuits whose responses matched the magnitudes and phases of the scattering parameters very well, but the resultant equivalent circuits, although valid, were not employed because they could not be related to the physical characteristics of the package since the circuit configuration was fixed by the algorithm and contained nonphysical elements.

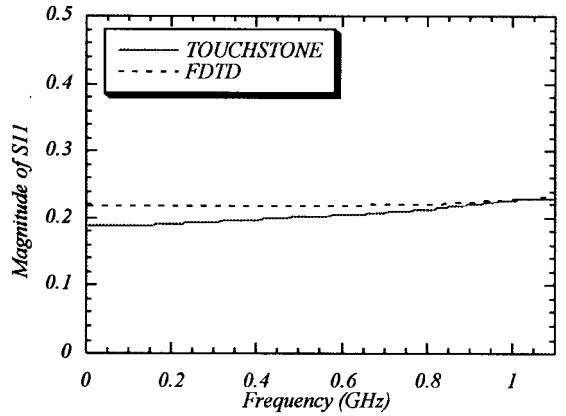
The magnitudes of the S-parameters for the rest of the cases are shown in Figs. 7(a)–9(b). For all of the cases, the frequency response of the equivalent circuit approximates that obtained from the FDTD analysis. We should add the remark that it is necessary to use the virtual ground model, shown in Figs. 2(c), 3(c), 4(c), and 5(c) and represented by elements L_4, C_3, and R_3 in Fig. 3(c), for example, to obtain the level of agreement seen in the S-parameters because this ground contributes a significant amount of inductance to the package model.

The lumped-circuit parameters for all of the cases examined are listed in Table I. This table can be used in conjunction with the equivalent-circuit diagrams to compare the circuit models for the various configurations. For example, it is obvious from these equivalent circuits that the level of coupling between the adjacent lines is considerably stronger than between those on opposite ends of the package.

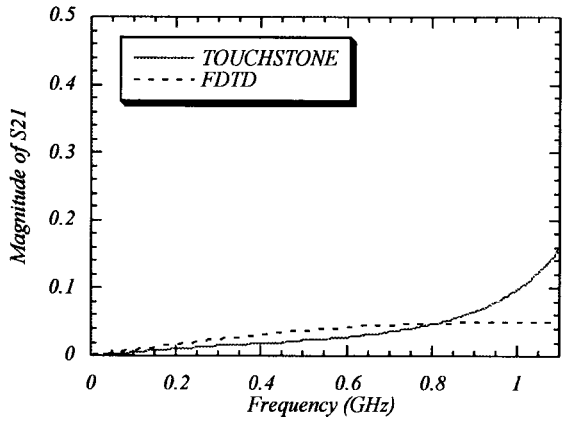
To use these equivalent circuits in circuit simulations of devices on the chip, the portions of the equivalent circuits labeled "via" are replaced with the device models, and then a circuit-simulation software such as SPICE is used. An important point to keep in mind about these circuits (developed with Touchstone) is that the accuracy with which they are able to model the internal ports at the silicon depends upon how well the internal electrical character is reproduced in the process of modeling the physical layout.

V. Conclusions

An FDTD–Touchstone hybrid technique has been employed in this paper for modeling the full-wave electromagnetic response of a complex silicon-chip package, in terms of passive RLC circuits. This approach allows the construction of equivalent circuits based on the package layout, which provide access to both the internal and external ports to the package even though the S-parameter model of the package, derived by using the FDTD method, did not contain explicit information corresponding to the internal ports. Since the development of the circuit branches for modeling the internal ports is based on physical layout considerations, we believe that the



(a)



(b)

Fig. 9. (a) Magnitude of S_{11} of Case D. (b) Magnitude of S_{21} of Case D.

circuit topology is reasonable; however, in practice it may be necessary to validate these by measurements. In any case, the agreement between the equivalent-circuit responses and the S-parameter data derived from the FDTD technique indicate that this methodology can lead to equivalent circuits which approximate the FDTD frequency response of the package in the frequency range of interest. For wide frequency ranges, a more automated process may be required to develop the equivalent circuit.

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